WHAT IS CLAIMED IS:

1. A non-volatile read only memory device, comprising:

a word line formed over a substrate, wherein the word line includes a metal layer and a polysilicon line;

a trapping layer located between the word line and the substrate; and

a polysilicon protection line formed over the substrate, the protection line electrically connects the word line and a grounded doped region in the substrate, wherein a resistance of the polysilicon protection line is higher than that of the word line.

2. The device of claim 1, wherein the resistance of the polysilicon protection line is higher than that of the polysilicon line of the word line.

3. The device of claim 1, wherein the polysilicon protection line is connected to the grounded doped region through a contact.

4. The device of claim 1, wherein the trapping layer includes a silicon oxide/silicon nitride/silicon oxide composite layer.

5. The device of claim 1, wherein the metal layer includes tungsten silicide.

6. The device of claim 1, wherein the polysilicon protection line is located above an isolation region.

7. The device of claim 6, wherein the isolation region include a field oxide layer.

8. The device of claim 1, wherein at least portion of the polysilicon protection line is formed over the grounded doped region.

9. A fabrication method for a non-volatile read only memory device, comprising:

forming a non-volatile read only memory cell on a substrate;

forming a polysilicon protection line on the substrate, the protection line is connected to a word line of the non-volatile read only memory cell, wherein a resistance of the polysilicon protection line is higher than that of the word line;

forming a grounded doped region; and

forming a contact on a substrate, the contact connects the grounded doped region and the polysilicon protection line.

10. The method of claim 9, wherein the method further comprises applying a high voltage to burn out the polysilicon protection line

11. The method of claim 9, wherein the polysilicon protection line is located on the substrate above an isolation region.

12. The method of claim 9, wherein at least a portion of the polysilicon protection line is formed above the grounded doped region.

13. A fabrication method for a non-volatile read only memory, comprising:

providing a substrate, the substrate comprises an isolation region;

forming a trapping layer on the substrate;

forming a polysilicon layer on the substrate;

forming a silicide layer on the polysilicon layer;

patterning the trapping layer, the polysilicon layer and the silicide layer to form a word line and a polysilicon line, wherein a dimension of the polysilicon line and the word line above the isolation region is smaller than that above other region;

removing the word line and a portion of the polysilicon line above the isolation region to form a polysilicon protection line, wherein a thickness of the polysilicon protection line is less than that of the polysilicon line;

forming a doped region in the substrate;

forming a first contact on the substrate, wherein the first contact connects the doped region and the polysilicon protection line; and

forming a second contact on the substrate, wherein the second contact connects the word line.

14. The method of claim 13, wherein the method further comprises applying a high current to burn out the polysilicon protection line.

15. The method of claim 13, wherein the trapping layer includes a silicon oxide/silicon nitride/silicon oxide composite layer.

16. The method of claim 13, wherein the metal layer includes tungsten silicide.

17. The method of claim 13, wherein removing the word line and the portion of the polysilicon line further comprising:

forming a patterned photoresist layer on the substrate, the patterned photoresist layer exposes a portion of the word line above the isolation region;

etching the exposed word line using the patterned photoresist layer as an etching mask;

continuously etching the polysilicon line under the word line to reduce a thickness of a part of the polysilicon line above the isolation region; and

removing the patterned photoresist layer.

18, The method of claim 13, wherein the isolation region includes a field oxide layer.

19. The method of claim 13, wherein at least a portion of the polysilicon protection line is formed above the doped region.